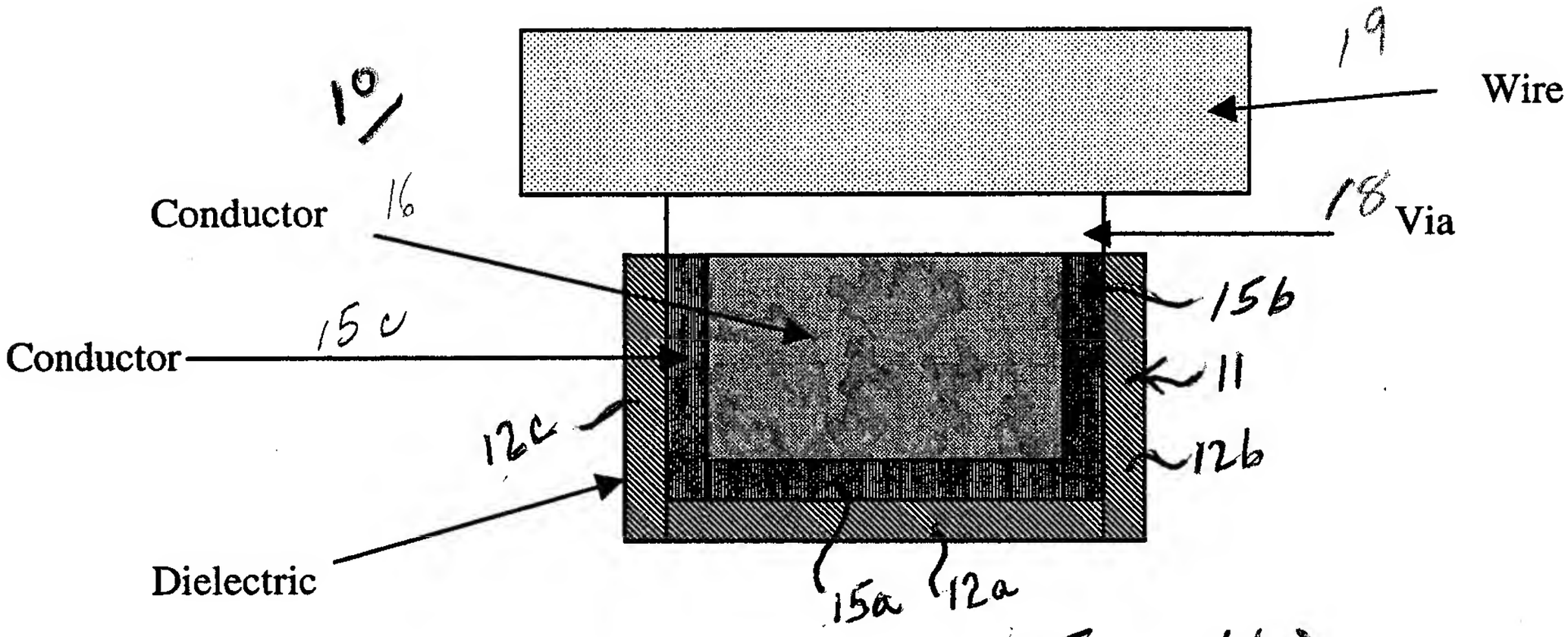
10
19
Wire
Conductor
16
18
Via
15b
Conductor
11
12c
12b
Dielectric
15a
12a

Fig 1(a)

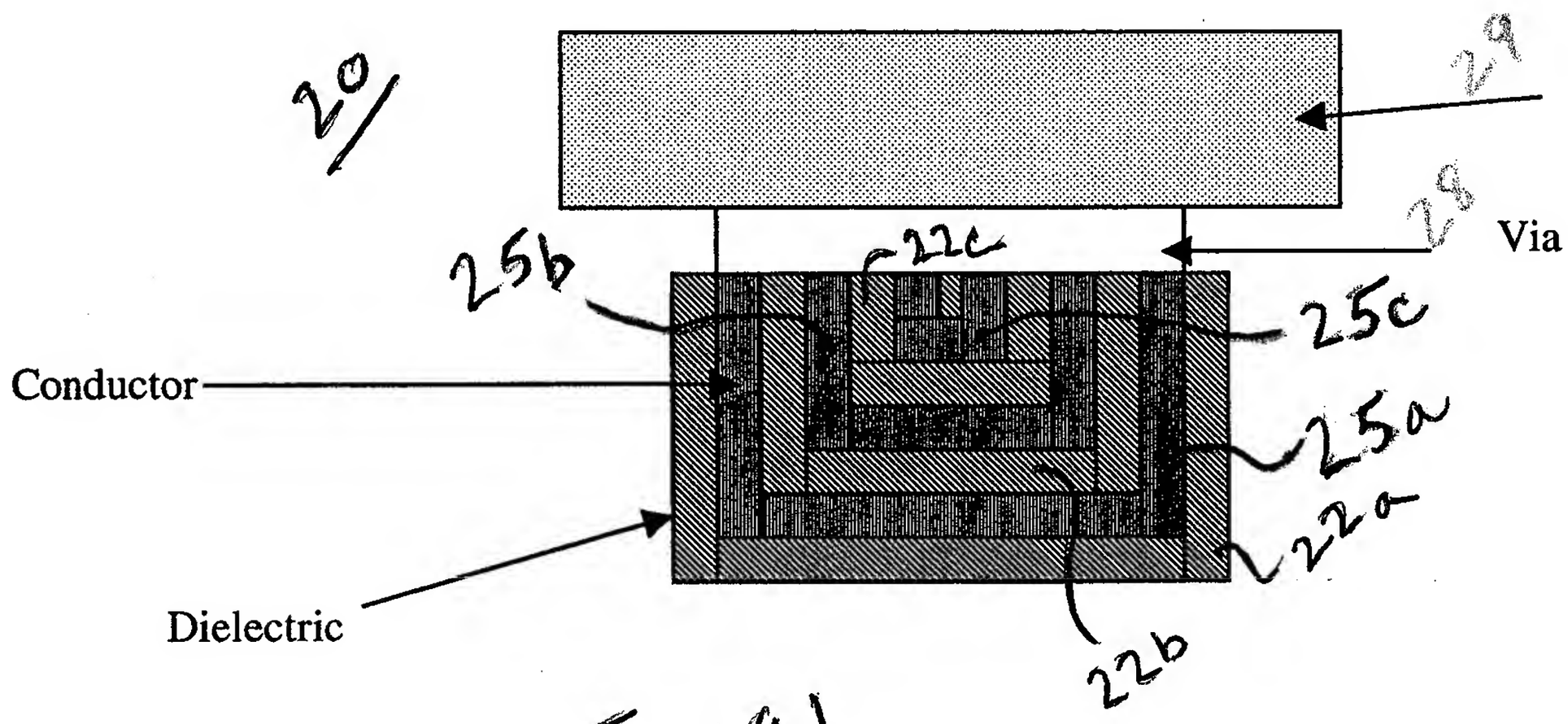
20
29
Wire
25b
22c
25c
Via
Conductor
25a
22a
Dielectric
22b

Fig 1(b)

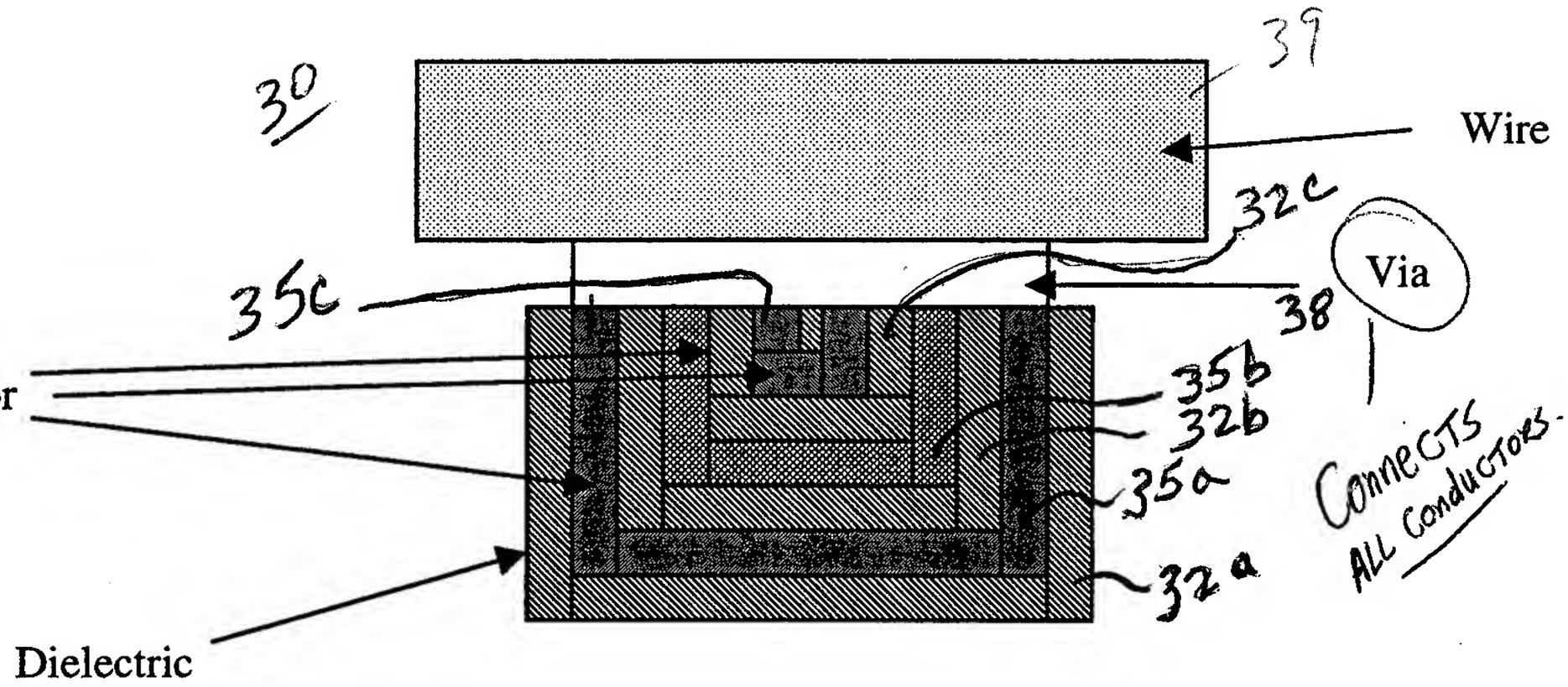
30
39
Wire
32c
35c
Via
38
Conductor
35b
32b
35a
Connects ALL Conductors
32a
Dielectric

Fig. 1(c)

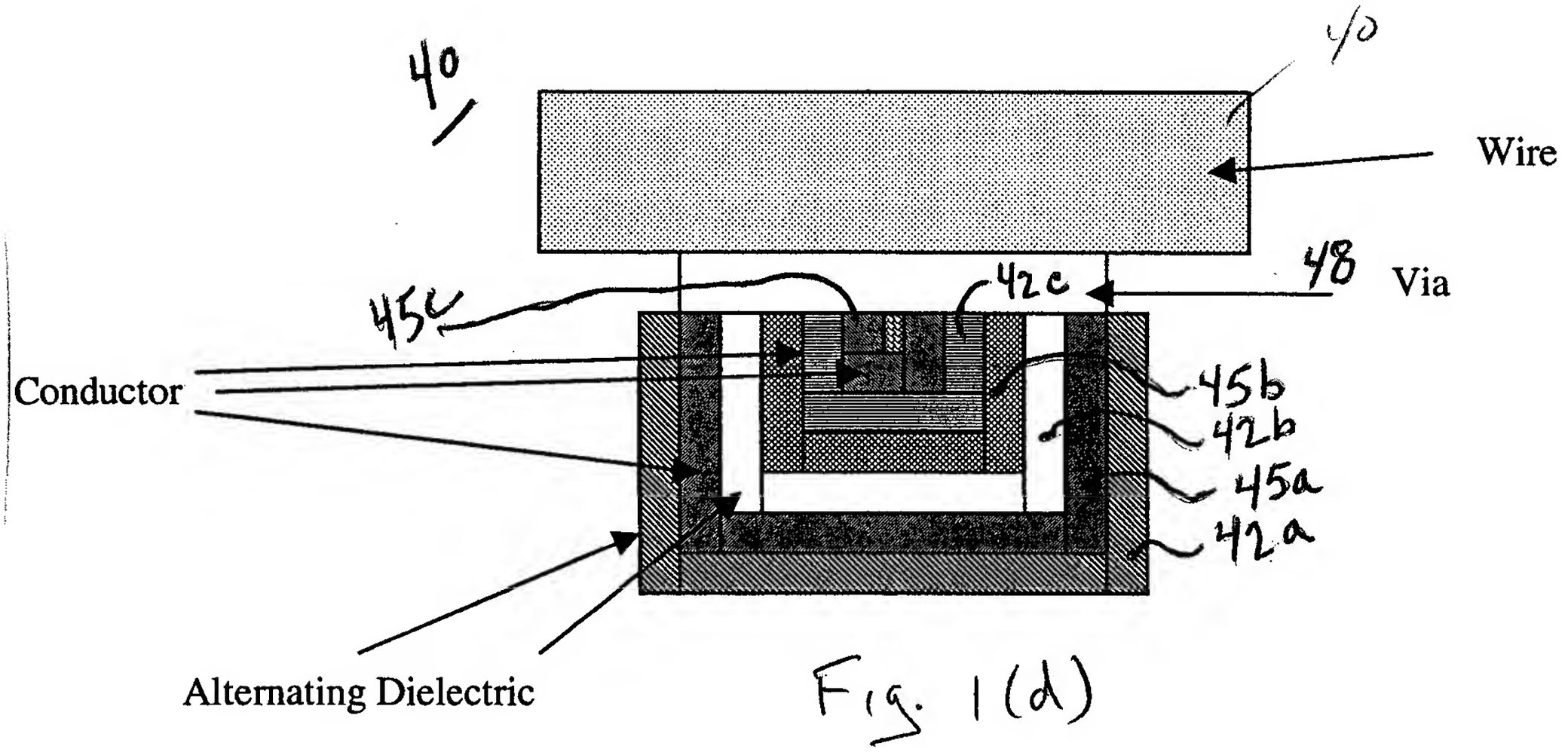
40
40
Wire
48
Via
42c
45c
Conductor
45b
42b
45a
42a
Alternating Dielectric

Fig. 1(d)

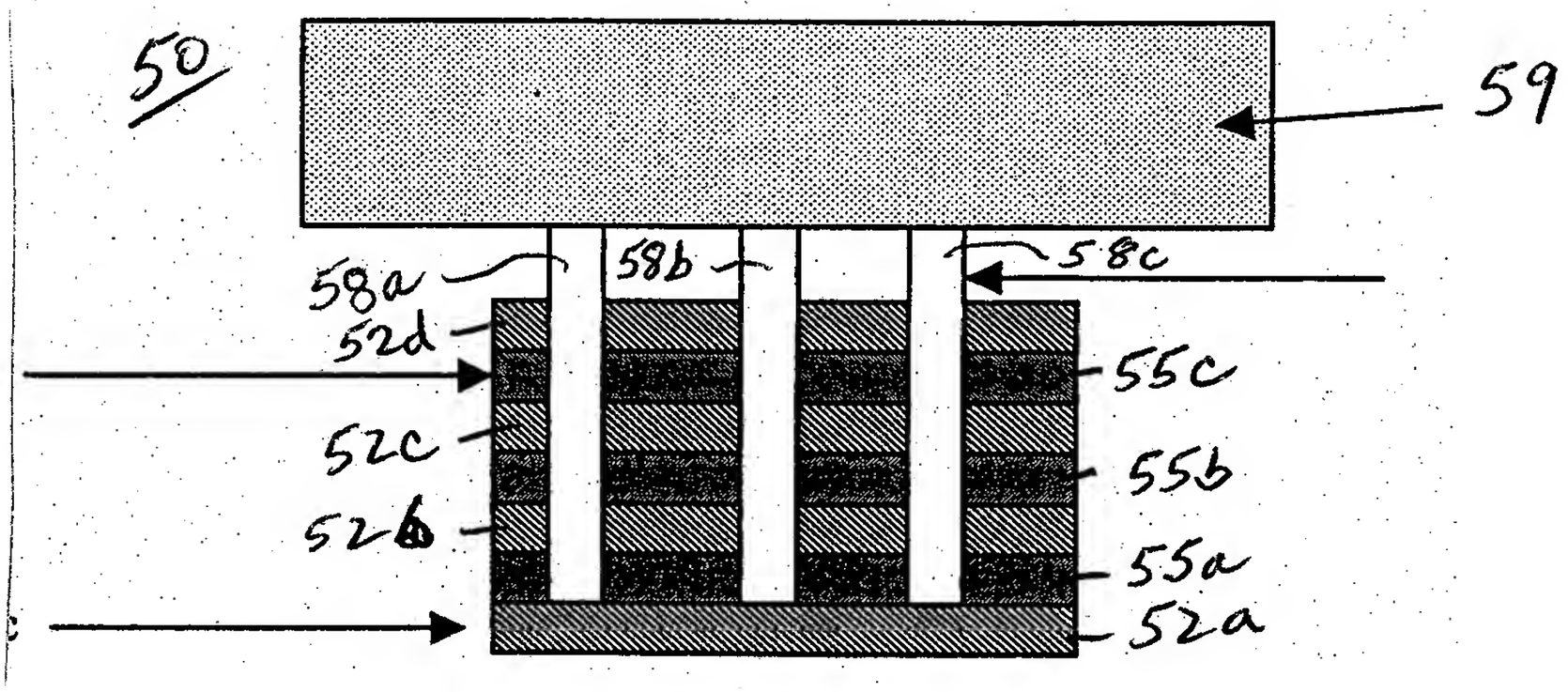
50
59
58a
58b
58c
52d
52c
52b
55c
55b
55a
52a

FIG. 2(a)

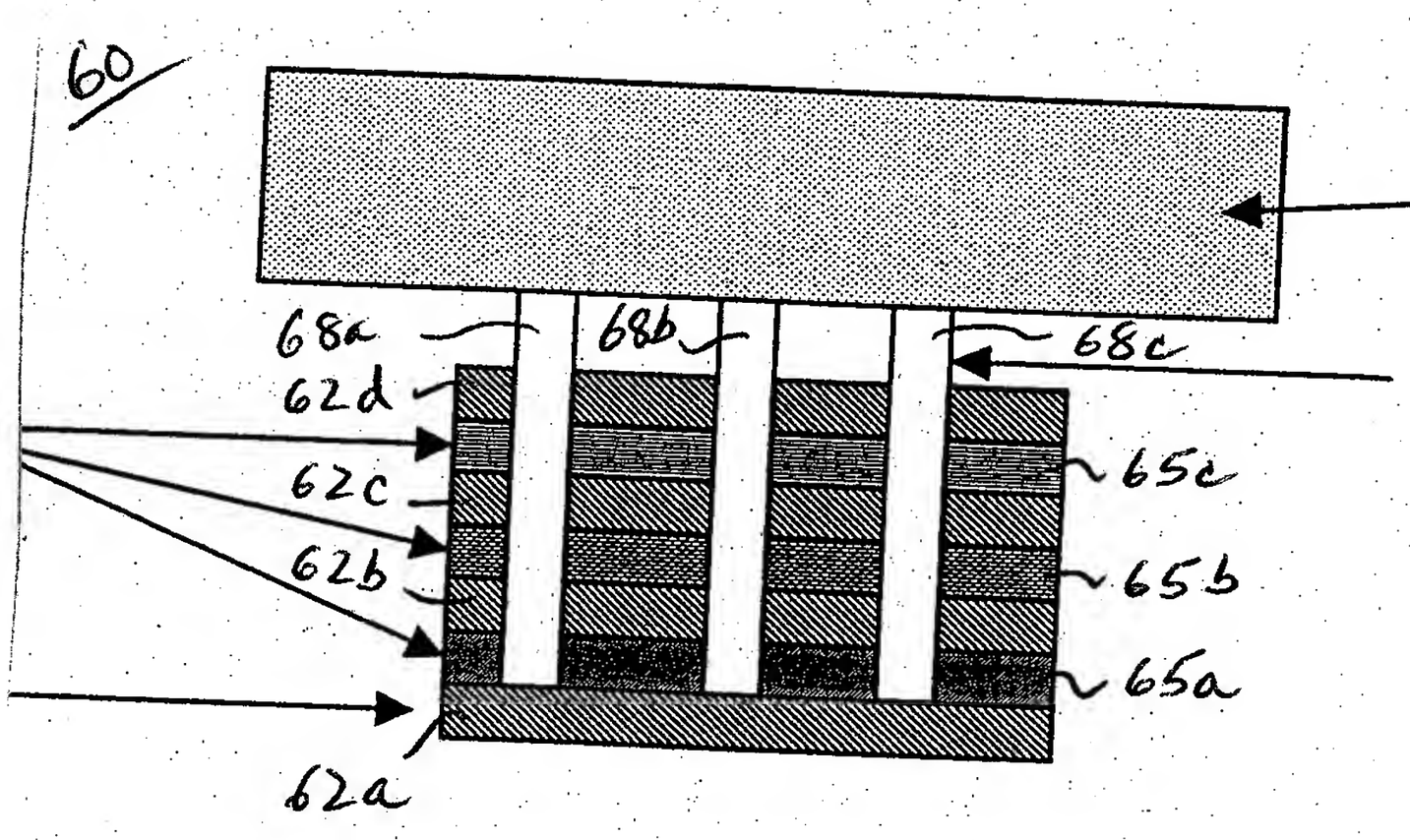
60
69
68a
68b
68c
62d
62c
62b
62a
65c
65b
65a

FIG. 2(b)

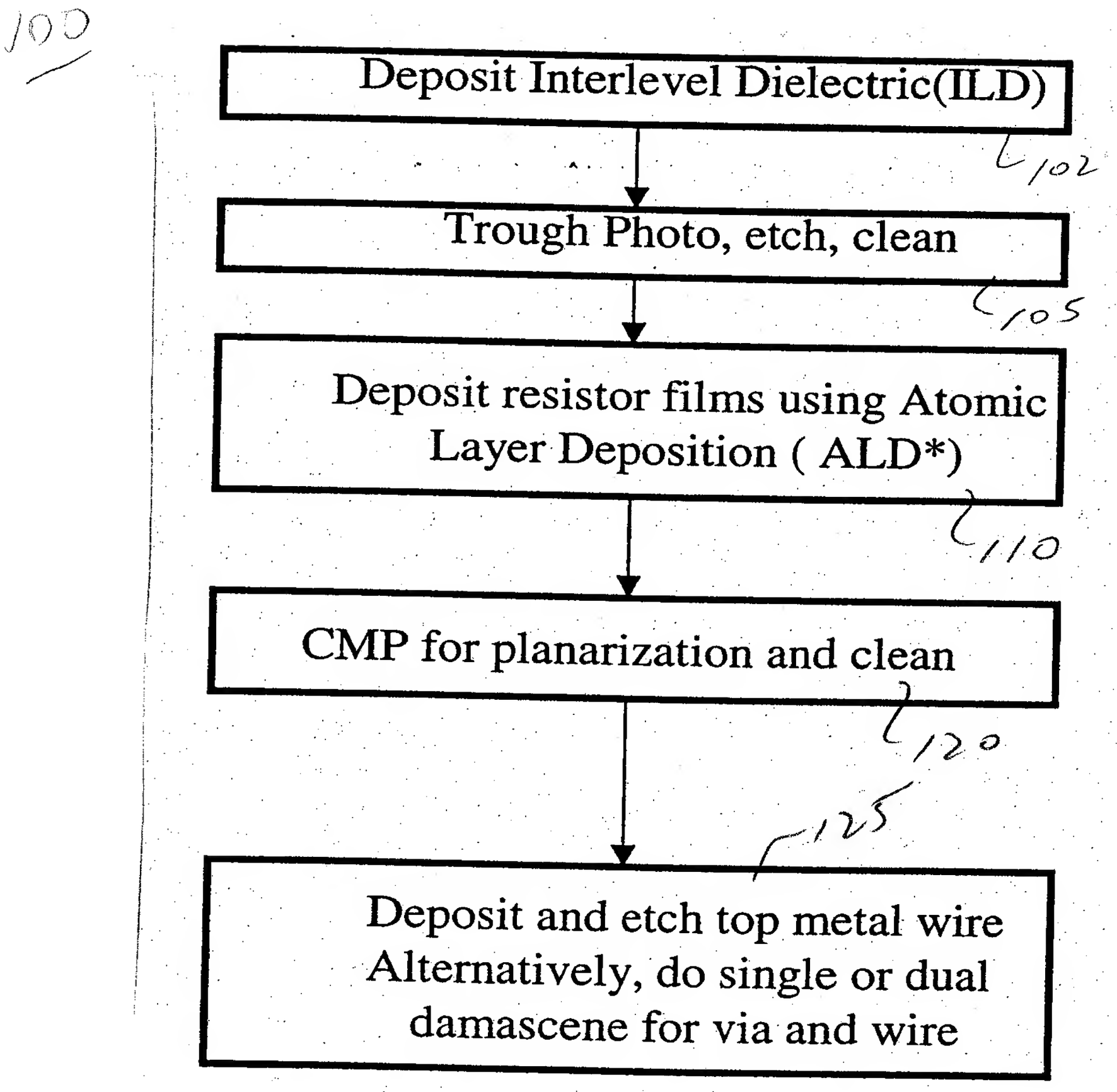
100
Deposit Interlevel Dielectric(ILD)
102
Trough Photo, etch, clean
105
Deposit resistor films using Atomic Layer Deposition (ALD*)
110
CMP for planarization and clean
120
125
Deposit and etch top metal wire
Alternatively, do single or dual damascene for via and wire

FIG. 3

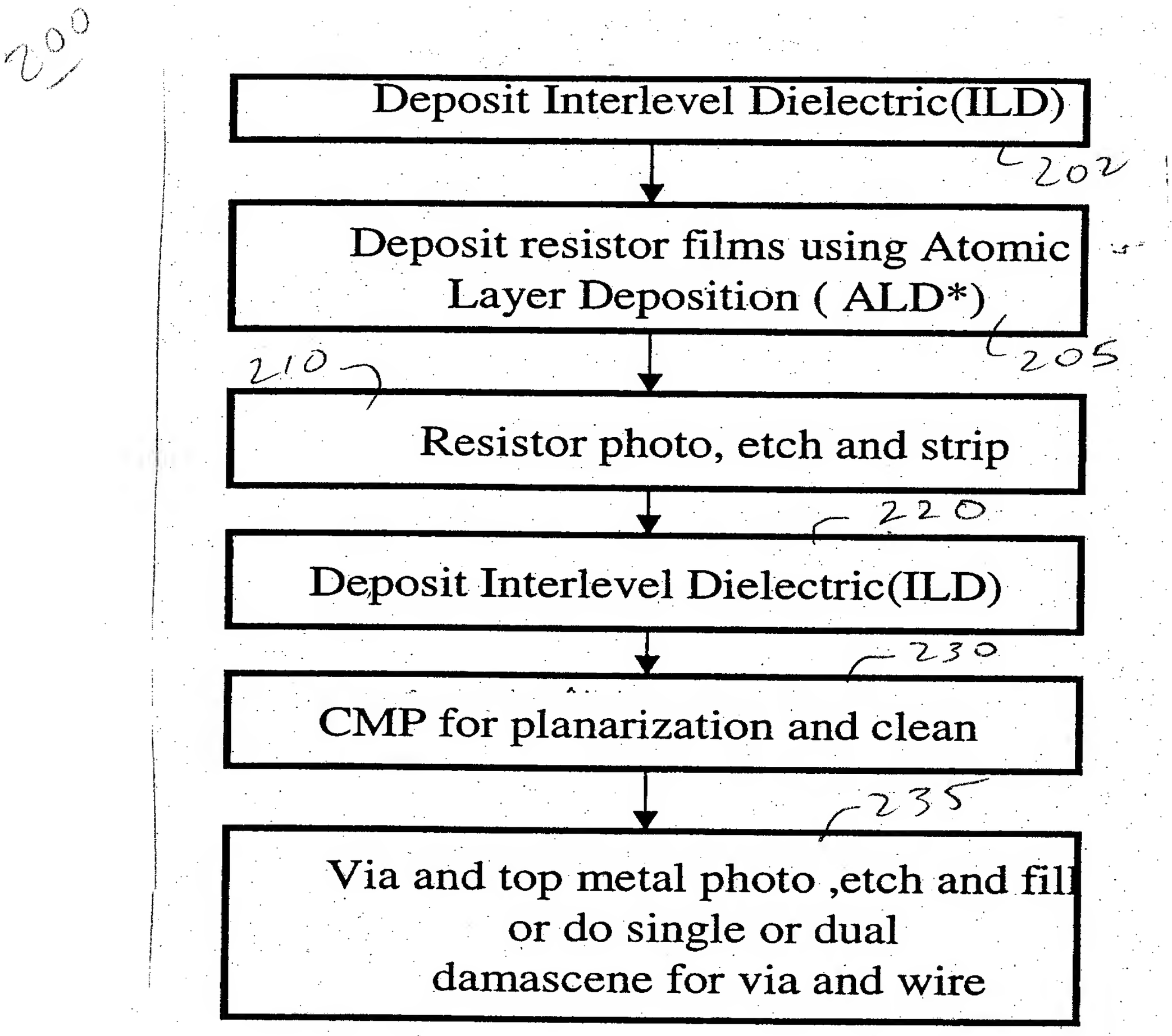
200
Deposit Interlevel Dielectric(ILD)
202
Deposit resistor films using Atomic Layer Deposition (ALD*)
205
210
Resistor photo, etch and strip
220
Deposit Interlevel Dielectric(ILD)
230
CMP for planarization and clean
235
Via and top metal photo ,etch and fill or do single or dual damascene for via and wire

FIG. 4

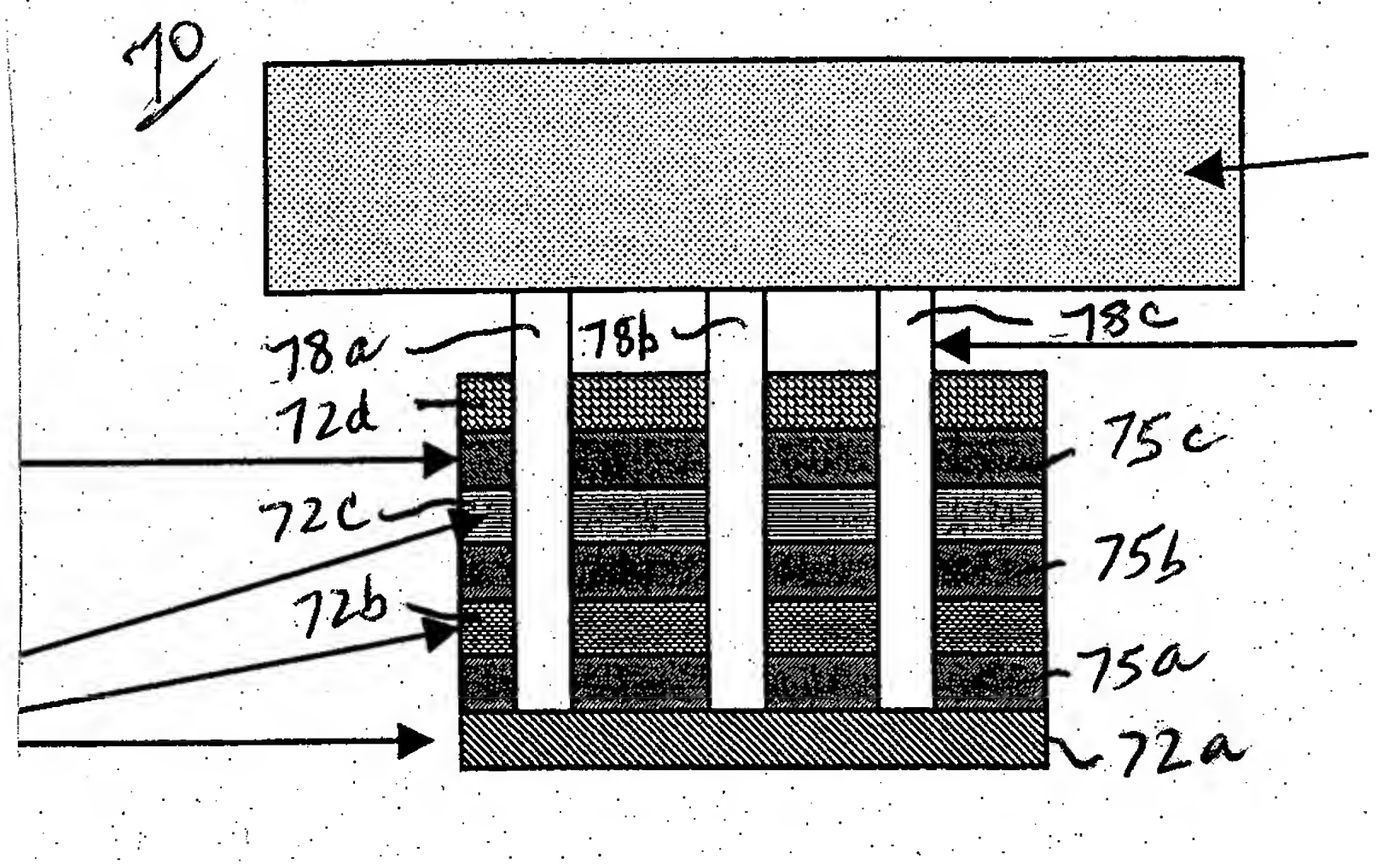
70
79
78a
78b
78c
72d
72c
72b
75c
75b
75a
72a

FIG. 2(c)

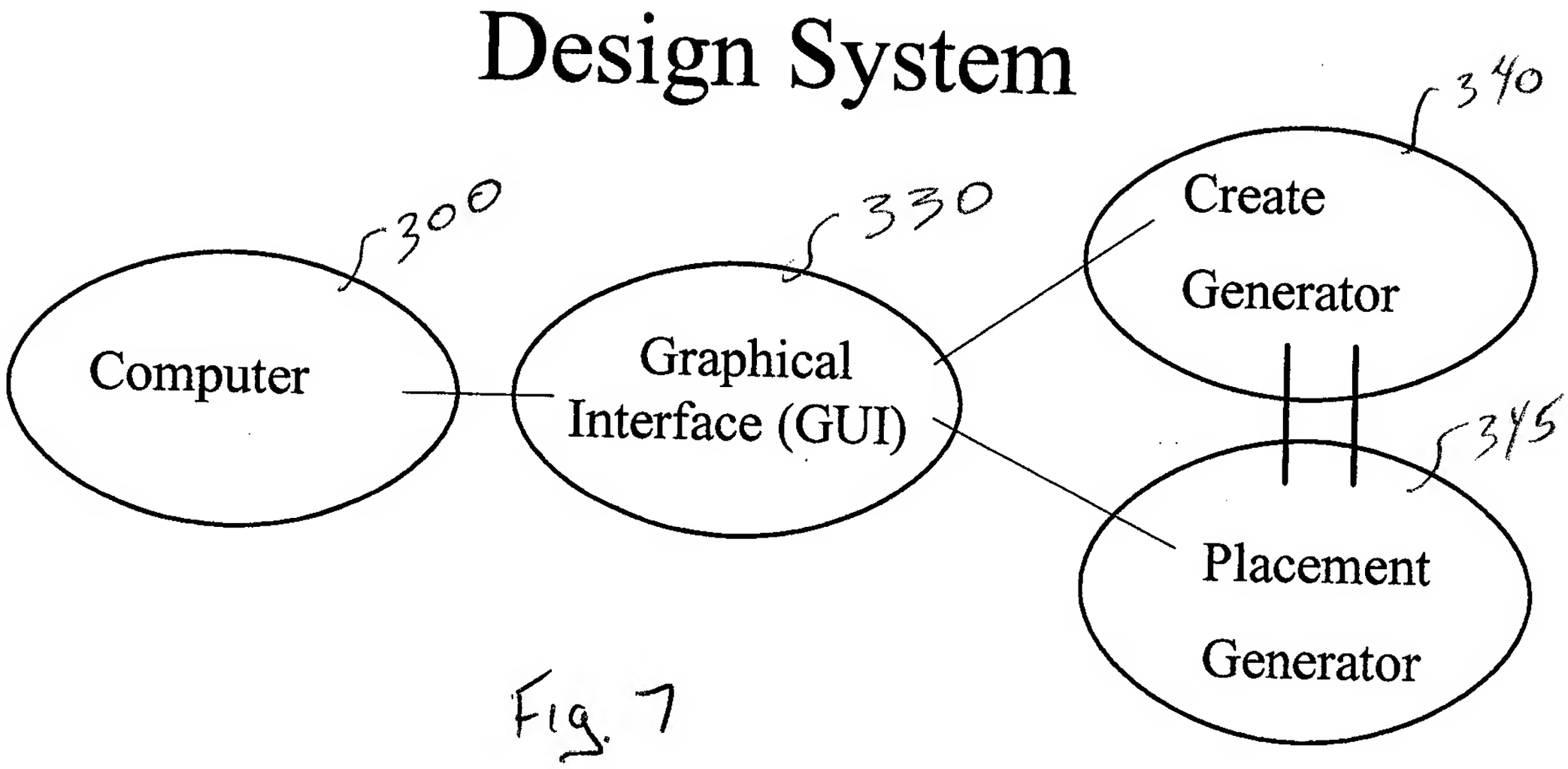
Design System
300
330
340
345
Computer
Graphical Interface (GUI)
Create Generator
Placement Generator

Fig. 7

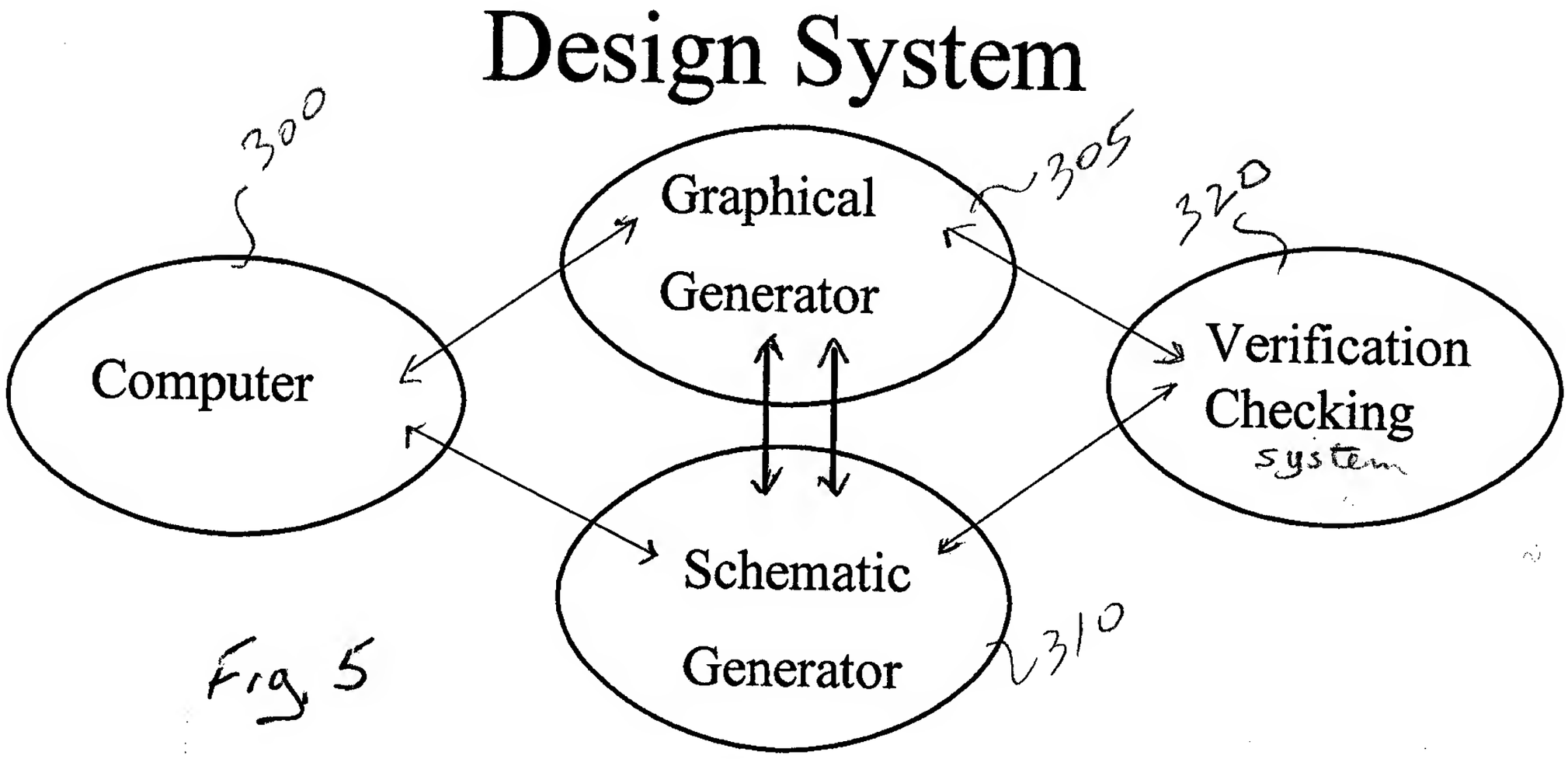
Design System
300
Graphical
Generator
305
320
Computer
Verification
Checking
system
Schematic
Generator
310

Fig 5

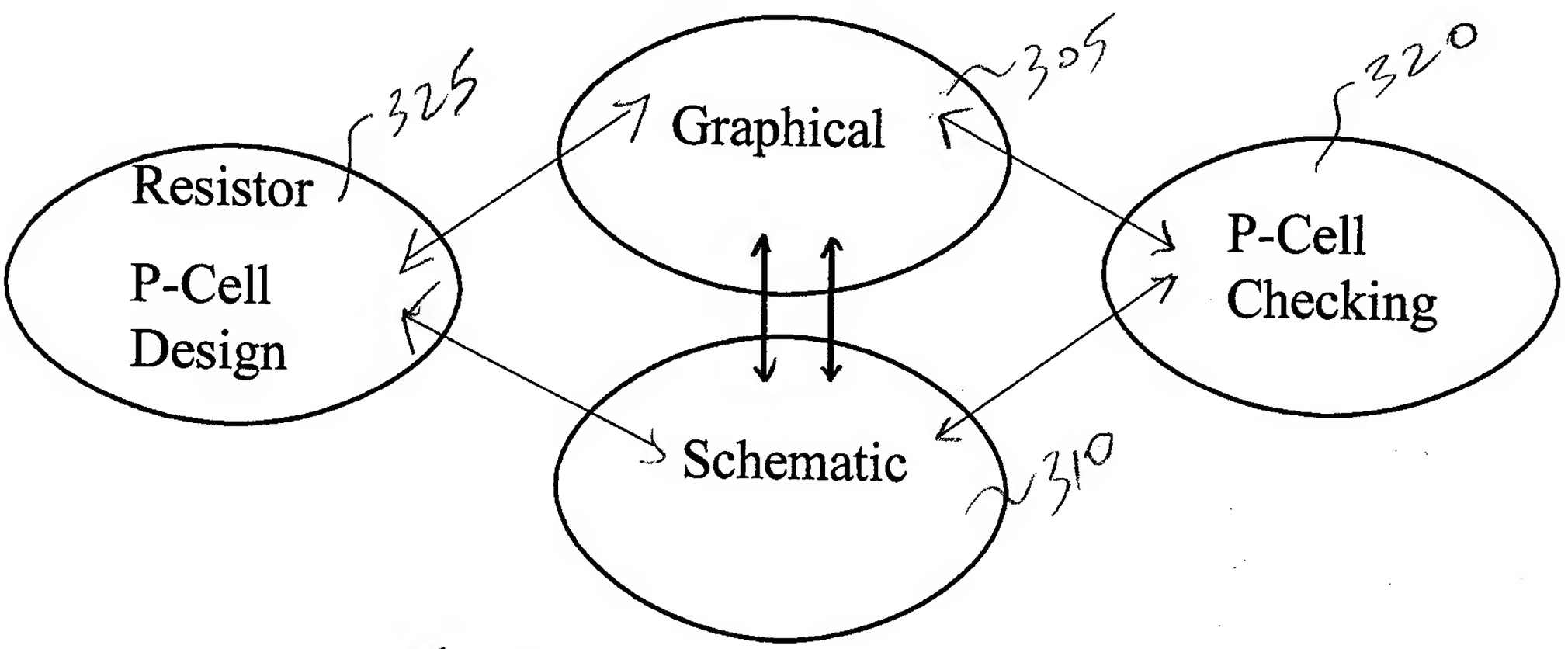
Design System
325
305
320
Graphical
Resistor
P-Cell
Design
P-Cell
Checking
Schematic
310

Fig. 6

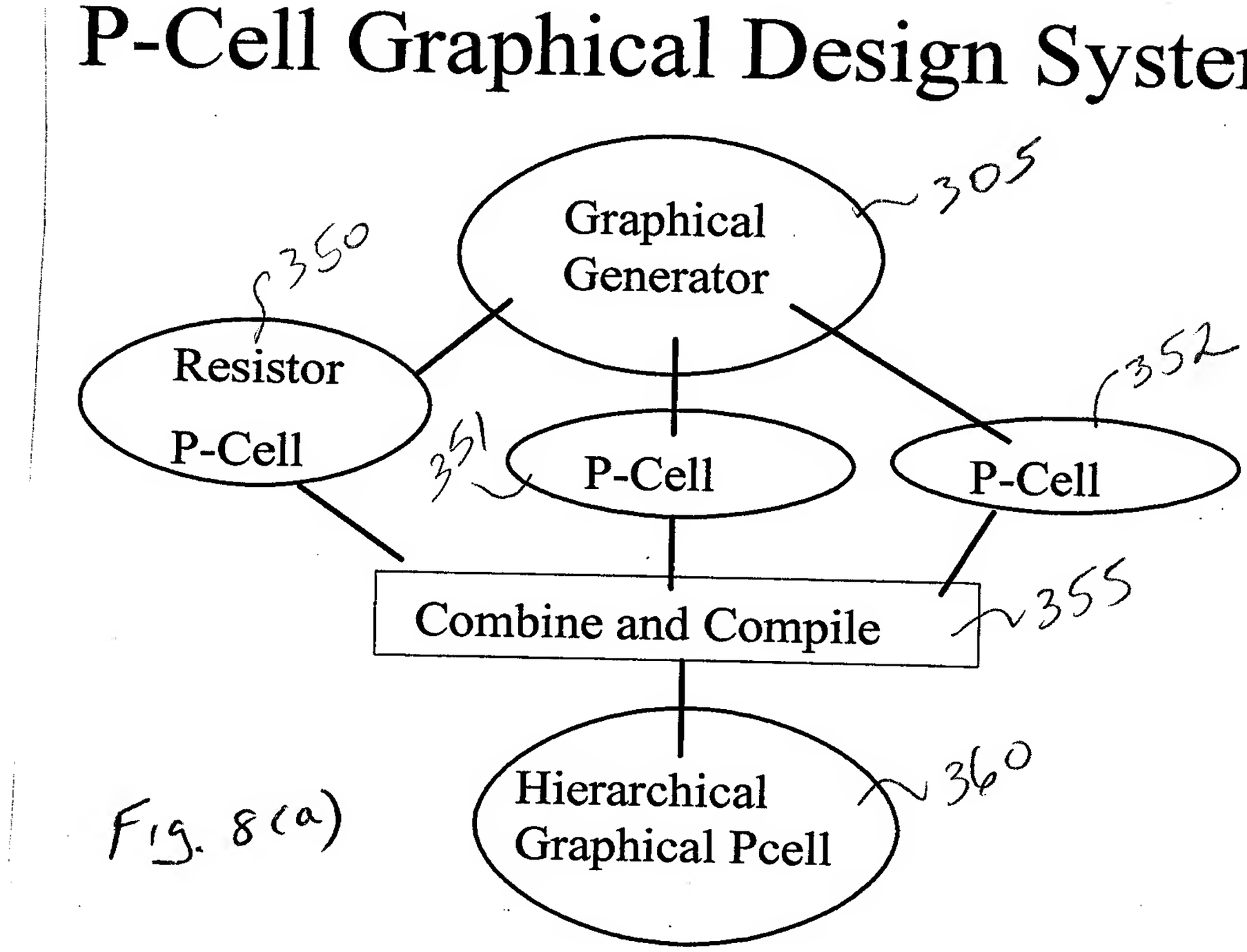
P-Cell Graphical Design System
Graphical Generator
305
350
Resistor P-Cell
351
P-Cell
352
P-Cell
Combine and Compile
355
Hierarchical Graphical Pcell
360

Fig. 8(a)

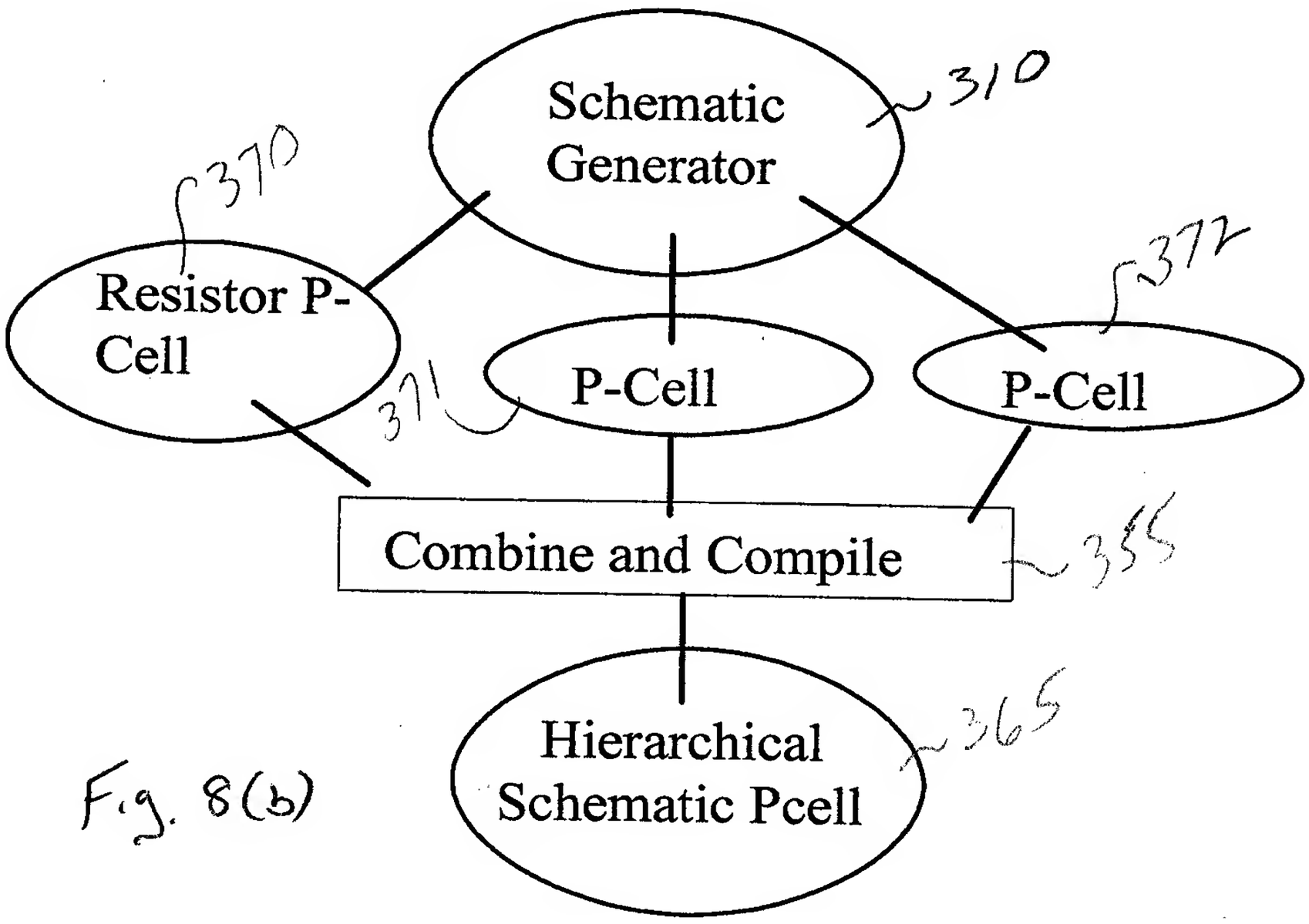
P-Cell Schematic Design System
Schematic Generator
310
370
Resistor P-Cell
371
P-Cell
372
P-Cell
Combine and Compile
355
Hierarchical Schematic Pcell
365

Fig. 8(b)

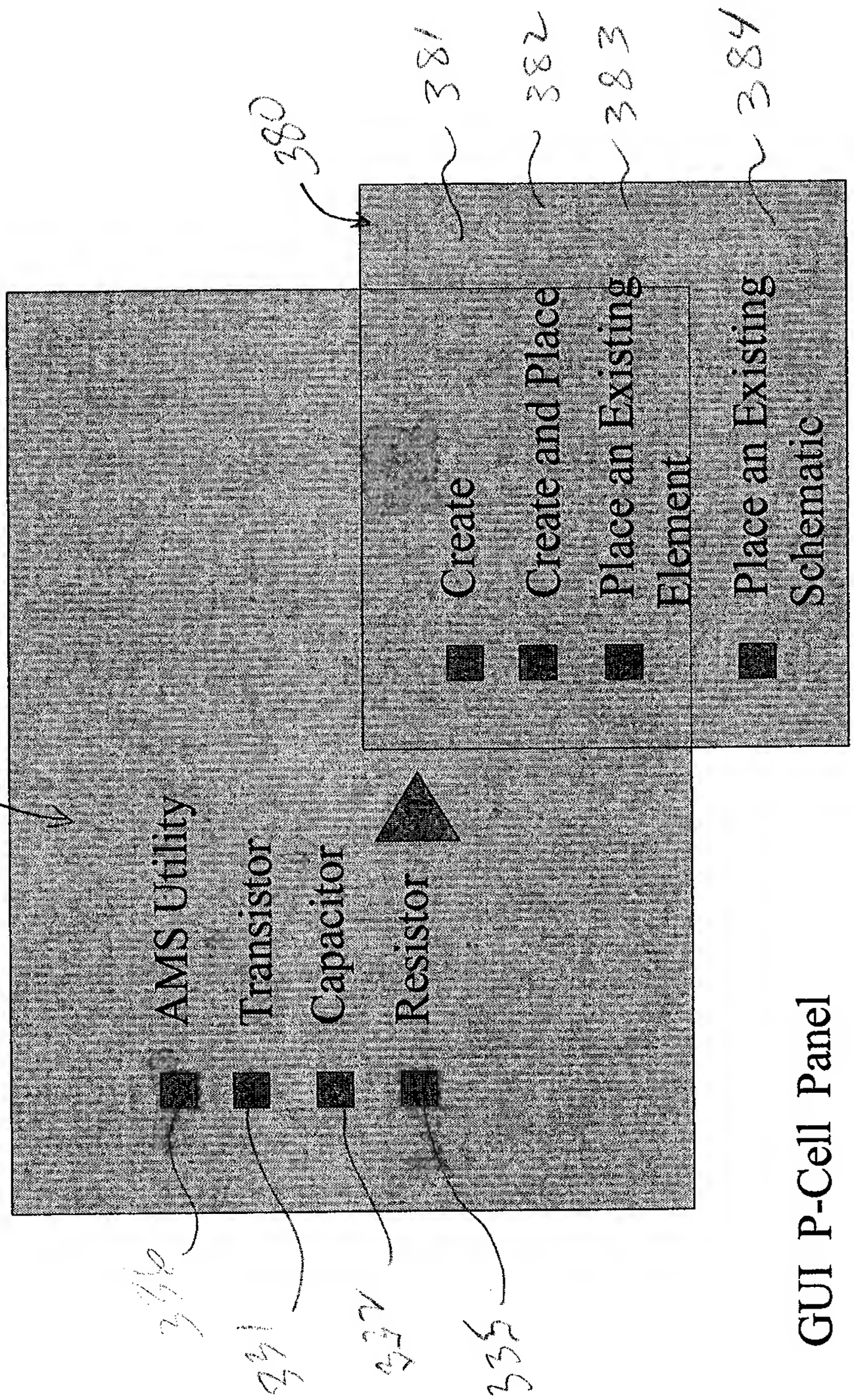
GUI P-Cell Panel
AMS Utility
Transistor
Capacitor
Resistor
Create
Create and Place
Place an Existing Element
Place an Existing Schematic
330
380
381
382
383
384
331
332
333
334
335

Fig. 9 (a)

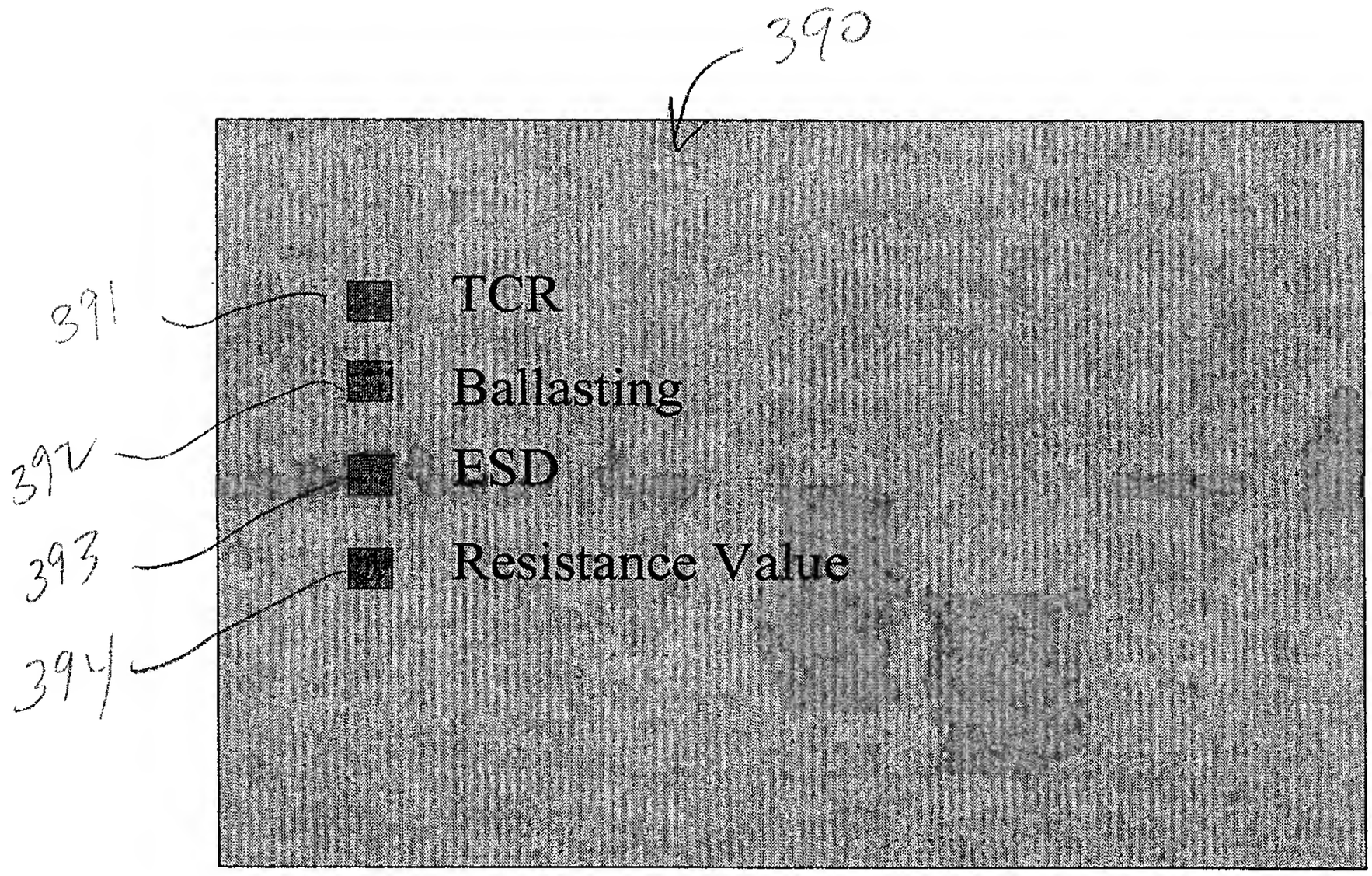

Fig. 9(b) Resistor P-Cell Panel

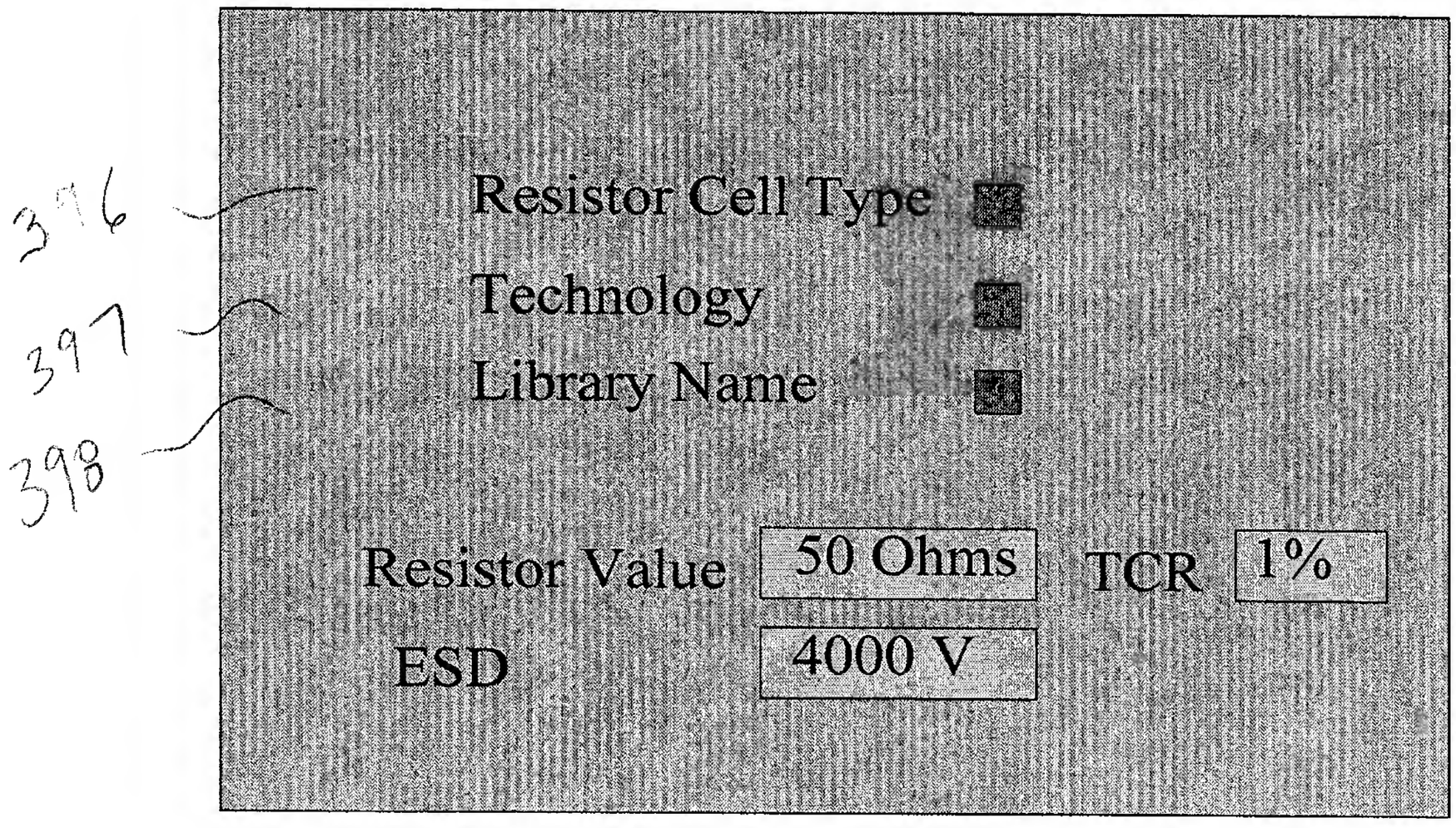

Fig. 9(c) Resistor P-Cell GUI Panel

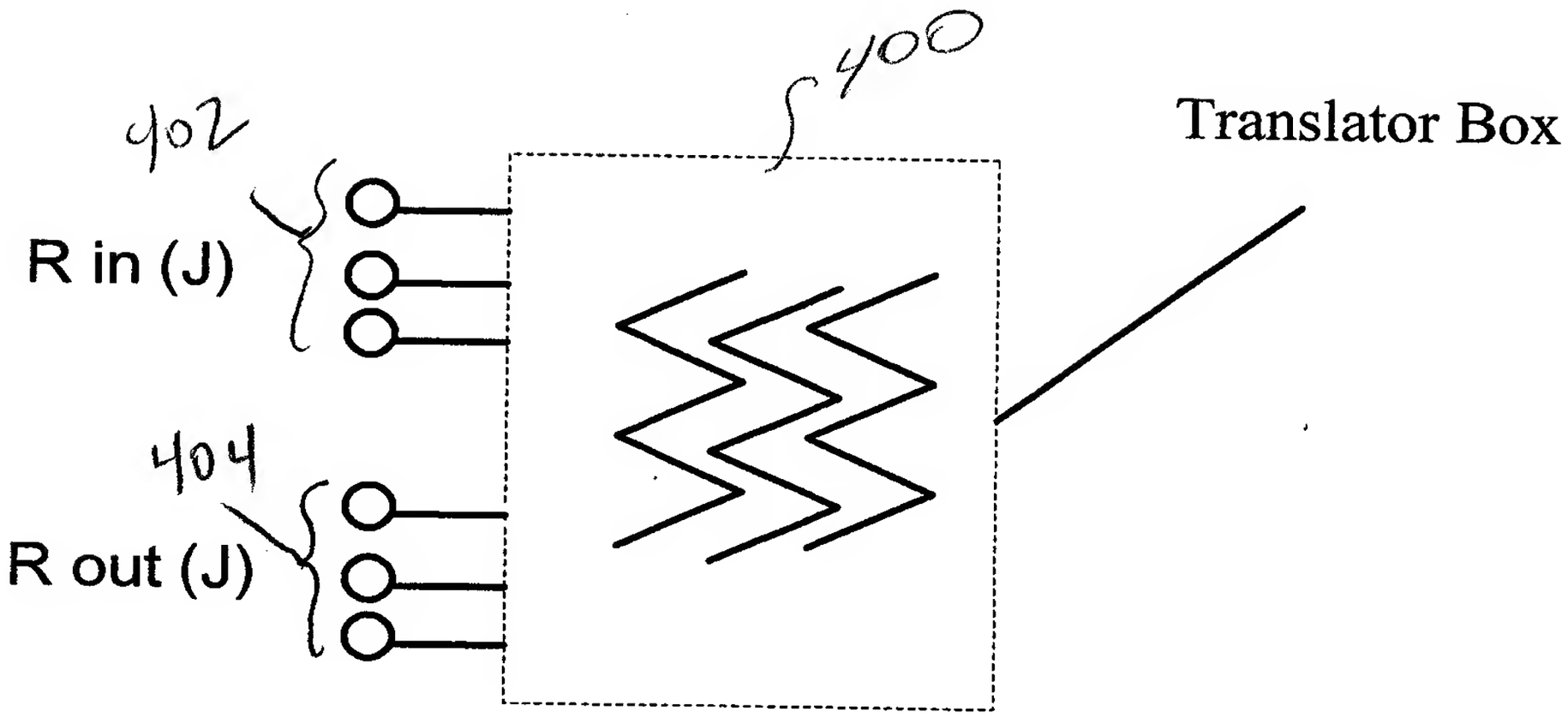

Fig. 10

Symbol Placement in Schematic Design

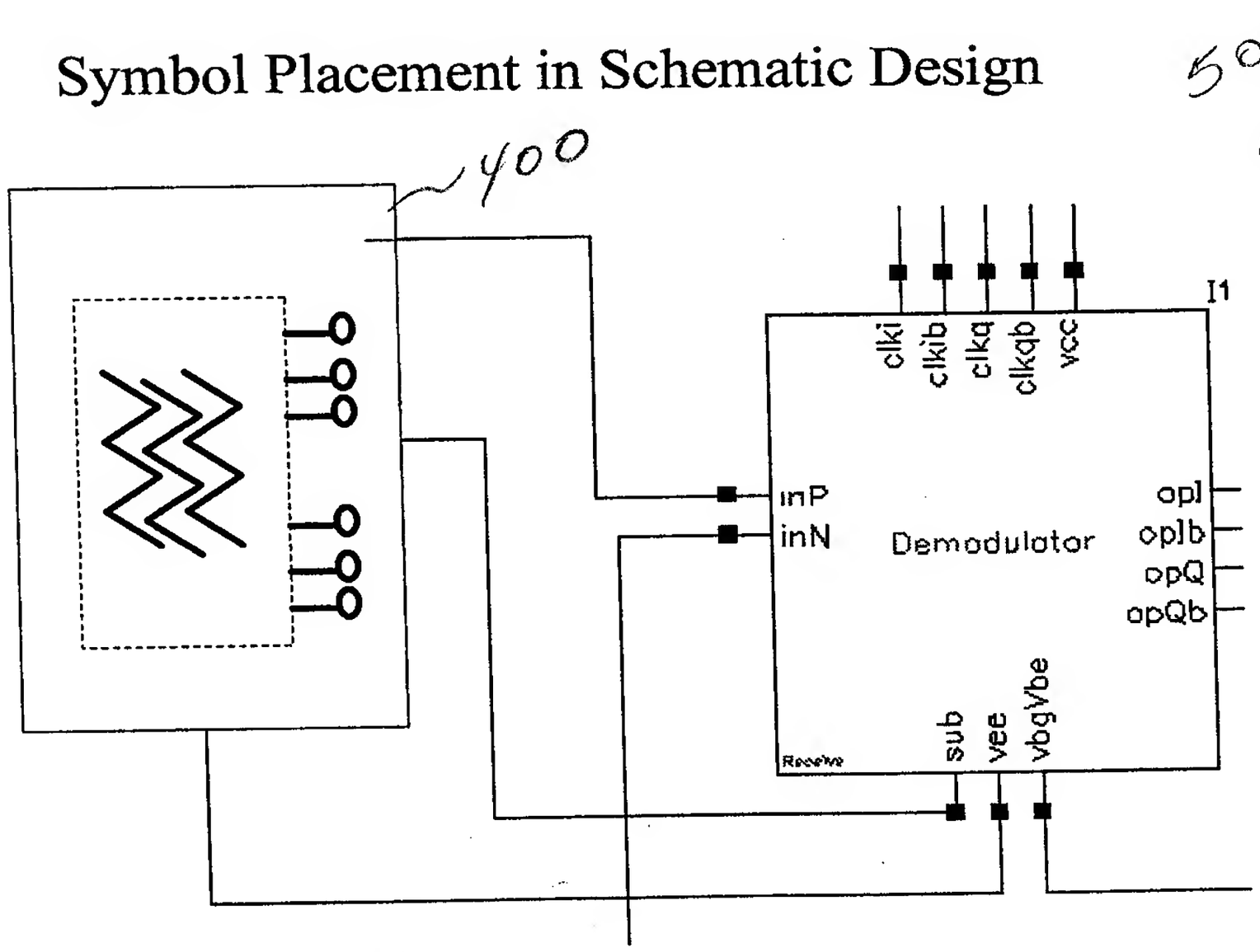

Fig. 11